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Patent Application

of

Serge PONTAROLLO
Résidence Saint André
Bâtiment D10
38800 Pont De Claix, FRANCE
Citizenship: FRENCH

for

CLAMP

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a clamp for protecting an integrated circuit against voltage surges which may occur between two terminals of the integrated circuit.

Voltage surges applied between two terminals of an integrated circuit can destroy the circuit. These voltage surges most often result from electrostatic discharges which can be inadvertently applied to the terminals of the integrated circuit in various circumstances. These circumstances may be a mere manipulation of the circuit by an operator whose fingers are brought to high electrostatic potentials by friction phenomena.

Discussion of the Related Art

Fig. 1 shows a conventional clamp 12. This device includes a bipolar NPN shunt transistor Q1 connected by its collector to terminal V^+ and by its emitter to terminal V^-. One or more Zener diodes 14 may be used to define the limit voltage between terminals V^+ and V^-, beyond which transistor Q1 turns on. The anode voltage of the Zener diodes 14 is applied to the base of transistor Q1 through a bipolar NPN follower transistor Q2. The bases of transistors Q1 and Q2 are connected to terminal V^- through respective resistors 18 and 19.

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With this configuration, transistor Q1 is turned on when the voltage between terminals V^+ and V^- becomes higher than the value Vz+2Vbe, where Vz is the sum of the voltages of Zener diodes 14 and 2Vbe is the sum of the base-emitter voltages of transistors Q1 and Q2.

Transistor Q1 is chosen with a particularly low on-resistance. It has a size of, for example, 300 elementary transistors. Follower transistor Q2 is used to supply a base current sufficient for transistor Q1 and includes for this purpose, for example, 100 elementary transistors.

A drawback of this clamp is the difficulty in obtaining a well known Zener voltage Vz. This Zener voltage must be higher than the nominal supply voltage of the circuit but must be lower than the maximum admissible voltage before circuit breakdown.

This range is relatively narrow and it often happens that, from the construction, the Zener voltage obtained is too low so that the clamp starts operating as soon as the circuit is normally supplied. It also often happens that, during circuit operation, by mere thermal drift or aging, the Zener voltage decreases and activates the clamp while the circuit is normally supplied.

Another drawback of this clamp is that transistor Q1 can be destroyed by a long voltage surge, which, however, is insufficient to damage the circuit the clamp protects. As a result, transistor Q1 is permanently short-circuited, which makes the circuit inoperable, even though it is in working order.

Most prior art clamps used in fast technologies are implemented by means of bipolar transistors. An electrostatic discharge has an almost vertical voltage leading edge followed by a progressive decrease. It is essentially this initial voltage value that must be reduced. For this purpose, the clamp must be able to react almost instantaneously. Up to now, it has not been possible to obtain an efficient clamp in slow CMOS technologies (for example, HC1PA).

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an efficient clamp for slow CMOS technology, which eliminates the problem of ensuring an accurate and stable triggering voltage.

To achieve this and other objects, the present invention provides a device for protecting a circuit against voltage surges, including a MOS transistor of a first type connected to first and second supply terminals by its source and its drain, respectively; a MOS transistor of a second type connected between the second supply terminal and the gate of the transistor of the first type, by its source and its drain, respectively; and a capacitor having a first terminal connected to the first supply terminal and a second terminal connected to the gate of the transistor of the second type.

According to an embodiment of the present invention, the device includes a reverse connected diode between the gate and the source of the transistor of the second type.

According to an embodiment of the present invention, the transistor of the first type is a P-channel transistor, the first supply terminal being a positive supply terminal.

These objects, features and advantages, as well as others, of the present invention will be discussed in detail in the following description of specific embodiments, taken in conjunction with the following drawings, but are not limited by them.

Brief Description of the Drawings

Fig. 1, previously described, shows a conventional clamp;

Fig. 2 shows an embodiment of a clamp which avoids the problem of ensuring a stable and accurate triggering voltage; and

Fig. 3 shows an embodiment of a clamp according to the present invention.

Detailed Description

Fig. 2 shows a clamp including, like the clamp of Fig. 1, a transistor Q1, controlled by a follower transistor Q2, for short-circuiting supply terminals V^+ and V^-.

According to an aspect of the invention, a capacitor C is connected between terminal V^+ and the base of follower transistor Q2 via, optionally, an NPN follower transistor Q3. Capacitor C and the base of transistor Q3 are connected to terminal V^- through a resistor 20. The base of transistor Q1 is connected to terminal V^- through a resistor 18, as in Fig. 1, and the base of transistor Q2 is connected to terminal V^- through a resistor 21.

With this configuration, the clamp is triggered, that is, transistor Q1 is turned on, when the voltage across resistor 20 becomes higher than 3Vbe (sum of the base-emitter voltages of transistors Q1 to Q3).

The voltage across resistor 20 essentially corresponds to the derivative of the voltage between terminals V^+ and V^-. Thus, the faster the voltage between terminals V^+ and V^- increases, the higher the voltage across resistor 20.

In an electrostatic discharge, capacitor C does not have the time to charge through resistor 20, that is, the base voltage of transistor Q3 increases at a rate similar to the voltage on terminal V^+. In this case, transistor Q1 is turned on almost as soon as the voltage between terminals V^+ and V^- becomes higher than 3Vbe, which results in eliminating a voltage surge.

Conversely, if the voltage between terminals V^+ and V^- increases relatively slowly, for example when the circuit being protected is normally turned on, the voltage across resistor 20 remains under 3Vbe and the clamp is not triggered.

When a permanent voltage surge is applied, the clamp is not triggered either, at least not after the voltage between terminals V^+ and V^- has reached a stable value. Therefore, transistor Q1 is not destroyed during permanent voltage surges which do not damage the circuit being protected.

The rate of the increase of voltage between terminals V^+ and V^- which triggers the clamp is determined by the values of capacitor C, resistor 20, the turn-on voltage (3Vbe in Fig. 2) of transistor Q1, and the gain of transistors Q1 to Q3. A rate is chosen, for instance, which is higher than the rate of increase during normal turn-on of the circuit being protected.

In order to adapt the clamp for use in slow CMOS technology, such as the HC1PA technology, the bipolar transistors of the structure of Fig. 2 could be replaced by MOS transistors. However, the device thus obtained has proven to be inefficient because the circuit it is supposed to protect is destroyed in most cases, under normalized test conditions (a 100 picofarads capacity charged at 2 to 4 kilovolts and discharged in the circuit through a 1500 ohms resistance). This inefficiency is due to the clamp's inability to react to a surge quickly enough. The efficiency of the MOS shunt transistor which replaces transistor Q1 directly depends on its gate-source voltage. However, this gate-source voltage is lower than one third of the voltage across resistor 20, which follows the voltage of a voltage surge. Therefore, the voltage surge will have time to destroy the circuit before this gate-source voltage reaches a sufficient value for the shunt transistor to absorb the voltage surge.

It has been found that, in CMOS technologies, bipolar NPN transistors with a vertical structure can be utilized, the only restriction being that the collectors of these NPN transistors correspond to the substrate, that is, to positive supply terminal V^+. The circuit of Fig. 2, with bipolar transistors, can thus be realized in pure CMOS technology. However, tests have shown that the clamp obtained in this manner still is too slow to be efficient, due to the low speed of vertical bipolar transistors.

Fig. 3 shows a clamp according to the present invention which is efficient even if implemented in slow CMOS technology. This device includes a P-channel MOS transistor MP connected between supply terminals V^+ and V^- by its source and its drain,

respectively. An N-channel MOS transistor MN is connected between the gate of transistor MP and terminal V^- by its drain and its source, respectively. The gate of transistor MN is connected to terminal V^+ through a capacitor C. The gate and the source of each of transistors MN and MP are interconnected through a resistor, respectively 20 and 22, which serves to discharge the gate-source capacitance of the transistor.

During a voltage surge, capacitor C does not have the time to charge through resistor 20, that is, the gate voltage of transistor MN increases at a rate similar to the voltage on terminal V^+. As soon as this gate voltage reaches the threshold voltage of transistor MN, transistor MN turns on and draws the gate voltage of transistor MP towards voltage V^-. Thus, transistor MP also turns on and short-circuits terminals V^+ and V^- to alleviate the voltage surge.

A reason for which the circuit of Fig. 3 is particularly fast is that the gate-source voltage of transistor MP quickly reaches a high value (equal to the circuit supply voltage) which makes it conductive enough to alleviate the voltage surge. Indeed, as soon as the gate voltage of transistor MN becomes greater than the transistor's threshold voltage by a given value, much lower than the value of the voltage surge, transistor MN enters a linear mode, that is, it behaves as a low value resistance, and brings the gate voltage of transistor MP almost back to voltage V^-. Transistor MN rapidly enters a linear mode, since the gate-source capacitance of this transistor constitutes, with capacitor C, a capacitive divider bridge which causes the gate voltage of transistor MN to vary proportionally to the voltage surge, the proportionality coefficient increasing with the increase of capacitor C.

In order to obtain a good compromise between the size of capacitor C and the turn-on speed of transistor MN, this transistor MN preferably is relatively small. As a result, transistor MN is not able to absorb the voltage surge which must be absorbed by the much larger transistor MP.

As an example, in a device according to the invention capable of absorbing voltage surges of 4 kV, transistor MN has a W/L ratio of 1,500/5, transistor MP a W/L ratio of 10,000/5, and capacitor C has a value of 8 picofarads. Resistors 20 and 22 have, for example, a value of 6 Kohms. If a voltage capacity of 2 kV is desired, the W/L ratio of transistor MP can be reduced to 5,000/5.

A device according to the invention, as that of Fig. 2, is triggered as soon as the voltage between terminals V^+ and V^- changes rapidly. As previously indicated, in the device of Fig. 2, the components are chosen so that the device is not triggered for a normal turn-on. However, the circuit's supply source generally has a particularly low impedance, which could cause the destruction of the clamp if the device should be triggered.

Despite a judicious selection of the components, it is always possible to encounter the case where a normal turn-on triggers the device, and causes its destruction if it is constituted by bipolar transistors. Indeed, a saturated bipolar transistor has a very low on-resistance, and regardless of the current flowing through it, this resistance decreases as the transistor heats up, which quickly tends to destroy the bipolar transistor.

Conversely, the fact that the clamp according to the invention, as shown in Fig. 3, formed with MOS transistors, triggers during normal turn-on, is not a nuisance. MOS transistor MP tends to behave as a current source with a value determined by its gate-source voltage. Thus, the current which flows through it never goes over this value and, as long as it is lower than this value, transistor MP behaves as a low value resistance. Further, a MOS transistor has a positive thermal coefficient which tends to decrease the current which flows through the transistor when its temperature increases. These combined characteristics make the clamp according to the invention particularly robust.

Alternatively, the types of transistors MN and MP can be reversed, by inverting the polarities of the supply terminals

V^+ and V^-. This has the advantage of reducing the surface occupied by the circuit, since the transistor which must bear the voltage surge is then an N-channel transistor which is approximately three times smaller than a P-channel transistor with the same characteristics. However, an N-channel MOS transistor has the disadvantage of having a parasitic bipolar transistor between its drain and its source. This parasitic bipolar transistor, bearing the current of the MOS transistor, decreases the robustness of the circuit because of its negative thermal coefficient.

As shown, a diode D is reverse connected between the gate and the source of transistor MN. This diode D prevents the gate voltage of transistor MN from becoming too negative with respect to voltage V^-. The gate voltage of transistor MN is equal to the voltage on terminal V^+ minus the voltage across capacitor C. Thus, if voltage V^+ quickly resumes its initial value, after a voltage surge, capacitor C does not have time to discharge through resistor 20, which causes a negative voltage surge between the gate and the source of transistor MN, which can lead to its destruction.

Of course, the present invention is likely to have various alterations and modifications, which will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The invention is limited only as defined in the following claims and equivalents thereto.

What is claimed is:

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